

FORM PTO-1449 (Colb)	ATTY DOCKET NO. 206,443	SERIAL NUMBER 10/774,169
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANTS' INFORMATION STATEMENT	APPLICANT Anat BREMLER BAR, et al.	EXAMINER (N/A)
	FILING DATE February 5, 2004	GROUP ART UNIT (N/A)



U.S. PATENT DOCUMENTS

Examiner's Initials		DOCUMENT NO.	DATE	NAME	CLASS	SUB	FILING DATE
TH	AA	6,397,335	05-2002	Franczek, et al.			
TH	AB	6,513,122	01-2003	Magdych, et al.			
TH	AC	2002/0083175	06-2002	Afek et al.			
	AD						
	AE						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB	TRANS- LATION
	AF						

OTHER ART (Including Author, Bills, Pertinent Pages, Etc.)

TH	AG	Bennett, J.C.R. et al. "Hierarchical Packet Fair Queueing Algorithms", 1996.
TH	AH	Bennett, J.C.R. et al. "High Speed, Scalable, and Accurate Implementation of Fair Queueing Algorithms in ATM Networks", 1996.
TH	AI	Bennett, J.C.R. et al. "WF2Q: Worst-Case Fair Weighted Fair Queueing", 1996.
TH	AJ	Chiussi, F.M. et al. "Implementing Fair Queueing in ATM Switches: The Discrete-Rate Approach", 1998.
TH	AK	Chiussi, F.M. et al. "Minimum-Delay Self-Clocked Fair Queueing Algorithm for Packet-Switched Networks", 1998.
TH	AL	Demers, A. et al. "Analysis and Simulation of a Fair Queueing Algorithm", 1989 Association for Computing Machinery.

EXAMINER: *Thompson*

DATE CONSIDERED: 4/9/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Colb)	ATTY DOCKET NO. 206,443	SERIAL NUMBER 10/774,169
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANTS' INFORMATION STATEMENT	APPLICANT Anat BREMLER BAR, et al.	EXAMINER (N/A)
	FILING DATE February 5, 2004	GROUP ART UNIT (N/A)

U.S. PATENT DOCUMENTS

Examiner's Initials		DOCUMENT NO.	DATE	NAME	CLASS	SUB	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB	TRANS- LATION
	AF						

OTHER ART (Including Author, Bills, Pertinent Pages, Etc.)

TH	AG	Eckhardt, D.A. et al. "Effort-limited Fair (ELF) Scheduling for wireless Networks", IEEE INFOCOM 2000.
TH	AH	Golestani, S.J. "Networks Delay Analysis of a Class of fair Queueing Algorithms", IEEE Journal on Selected Areas in Communications, Vol. 13, no. 6, August 1995, pp. 1057-1070.
TH	AI	Golestani, S.J. "A self-Clocked fair Queueing Scheme for Broadband Applications", IEEE 1994, pp. 5c.1.1-5c.1.11.
TH	AJ	Greenberg, Albert G. et al. "How Fair is Fair Queueing?" Journal of the Association for Computing Machinery Vol. 39, no. 3, July 1992, pp. 568-598.
TH	AK	Parekh, A.K.J. "A Generalized Processor Sharing Approach to Flow Control in Integrated Services Networks", Ph.D. Dissertation Massachusetts Institute of Technology, February 1992.
	AL	Parekh, A.K.J. "A Generalized Processor Sharing Approach to Flow Control in Integrated Services Networks: The Multiple Node Case", IEEE/ACM Transactions on Networking Vol. 2, no. 2, April 1994, pp. 137-150.

EXAMINER: *Thurmon*

DATE CONSIDERED: 4/9/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Colb)	ATTY DOCKET NO. 206,443	SERIAL NUMBER 10/774,169
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANTS' INFORMATION STATEMENT	APPLICANT Anat BREMLER BAR, et al.	EXAMINER (N/A)
	FILING DATE February 5, 2004	GROUP ART UNIT (N/A)

U.S. PATENT DOCUMENTS

Examiner's Initials		DOCUMENT NO.	DATE	NAME	CLASS	SUB	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB	TRANS- LATION
	AF						

OTHER ART (Including Author, Bills, Pertinent Pages, Etc.)

TH	AG	Parekh, A.K.J. "A Generalized Processor Sharing Approach to Flow Control in Integrated Services Networks: The Single-Node Case", IEEE/ACM Transactions on Networking Vol. 1, no. 3, June 1993, pp. 344-357.
TH	AH	"Quality of Service Networking", downloaded from the web (address: http://www.cisco.com/univercd/cc/td/doc/cisintwk/ito_doc/qos.htm), Cisco Systems, Inc. 2002.
TH	AI	Rexford, J.L. et al. "Hardware Efficient Fair Queueing Architectures for high-Speed networks", IEEE 1996, pp. 5d.2.1-5d.2.9.
TH	AJ	Shreedhar M. et al. "Efficient Fair Queueing Using Deficit Round-Robin", IEEE/ACM Transactions on networking Vol. 4, no. 3, June 1996, pp. 375-385.
TH	AK	Stiliadis, D. et al. "Frame-Based Fair Queueing: A New Traffic Scheduling Algorithm for Packet-Switched Networks", July 1995, pp. 1-43.
	AL	
EXAMINER: <i>Throglou</i>		DATE CONSIDERED: 4/9/06
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		